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HYBRID VLSI ARCHITECTURE FOR HIGH-RESOLUTION IMAGE PROCESSING

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Abstract - High-resolution image processing needs have increased in applications that involve medical diagnostics along with satellite imaging and real-time video surveillance and autonomous systems. Real-time operation must be achieved alongside minimum power usage to maintain superior image quality in current programming scenarios. A new VLSI architecture emerges which joins ASIC and FPGA technology advantages to attain optimization of high-resolution image processing operations. The architecture implements two stages of data processing through a combined ASIC and FPGA framework which positions these hardware elements to handle specific computational and adaptive and parallel tasks. The solution method leads to faster processing alongside lower power usage and shorter latency periods along with no reduction in image quality. Experimental testing indicates that the proposed system reaches 60 frames per second (FPS) processing speed coupled with 150 mW power consumption and 20 millisecond latency alongside 180 megapixels per second (MPixels/s) throughput achievement. The proposed approach delivers exceptional image quality performance as shown by PSNR metric of 38.5 dB and SSIM of 0.92. The new proposed structure offers superior performance compared to ASIC-only and FPGA-only and hybrid VLSI designs and emerges as a favorable technology for high-resolution real-time imaging applications.

Keywords - Low Power Consumption, ASIC and FPGA Integration, Dual-Stage Pipeline, Parallel Processing, Image Quality Enhancement, Latency Reduction

I. INTRODUCTION

Different sectors such as medical diagnostics and satellite image analysis together with autonomous vehicles and real-time video surveillance and industrial automation experienced fundamental transformation through high-resolution imaging technologies' rapid proliferation. Real-time processing and power efficiency together with processing accuracy constitute vital requirements for these applications. Current software methods for image processing encounter major limitations when dealing with rising image definitions and growing data sets because they struggle to fulfill real-time processing needs. Software systems operating purely through programming fail to meet power efficiency standards and performance requirements when executed on GPUs especially in embedded processing systems. ASIC-based image processing architectures operate efficiently but cannot change to new processing algorithms or handle shifting computational requirements. The ability of FPGA systems to reconfigure and operate in parallel comes with difficulties to reach sufficient power efficiency needed for sustained real-time processing tasks in limited resource environments.

These performance issues can be solved by implementing VLSI hybrid systems which unite ASIC modules with FPGA hardware. By using ASIC along with FPGA a system becomes capable of using each technology's advantages where ASIC performs resource-intensive image processing quickly at low power while FPGAs enable real-time adaptable operations. These combined hardware systems handle different image processing operations efficiently with their ability to process simple computations and elaborate pattern recognition duties. Although, there is a lot of work done in VLSI-based image processing, so far architectures in literature mainly deals with either speed optimization or power optimization. Very few designs succeed in combining both characteristics

and providing flexibility for various image processing operations. This paper fills this gap by suggesting a new hybrid VLSI architecture which has the ability to efficiently interleave ASIC and FPGA techniques for realizing high performance and low power processes for high quality image handling.

The proposed architecture uses a dual stage pipeline where ASIC modules carry out core analyzations, for example, convolution, edge detection, image enhancement. Meanwhile, FPGA modules dynamically schedule adaptive resolution and real-time processing requests. A high-speed communication interface enables easy data exchange between ASIC and FPGA boards with minimal latency and maximum throughput. Performance evaluation results on high-resolution medical and satellite image datasets shows that the proposed architecture achieves a better processing rate while achieving, and significantly reduce the power consumption versus designs. Furthermore, the hybrid architecture is capable of being extended to emerging image processing methods and applications thanks to the modular nature of the architecture.

II. LITERATURE SURVEY

High resolution Image processing finds extensive application in numerous areas of research & developments with remedial application areas being Medical images analysis and Satellite images processing as well as complying Real time Surveillance. The problem is to get competitive real-time performance with low power of the system. The traditional VLSI-based architectures have been studied profoundly in order to improve the processes of image treatment. Some architectures achieved low power consumption by means of clock gating and power efficient convolution but, they lack the decision to handle with adaptive image processing applications [1], [2]. However, where to go? FPGA-based architectures provide reconfigurability and parallelism and they are able to process image processing tasks efficiently. However, they usually have the deficiency of boost error consumption and scalability for processing ultra-high-resolution images [3], [4].

To date such limitations, Hybrid VLSI architectures (ASIC + FPGA) are receiving increasing attention for time-to-market customized system applications. These hybrid designs combine speed and power efficiency of ASICs, packaging power of FPGA. There are a few studies that proposed the hybrid architecture for the medical image compression and edge detection, showed enhanced processing speed but usually loading with the resolution scalability and power saving [5, 6]. There have also, more recently, been approaches that embedded deep learning accelerators in hybrid architectures to improve the performance but pull very high loads of power side of complex image transforms [7], [8].

In the recording shipments of real-time image processing, in addition to high-speed of the processing, with efficient improvements in power management is required. A number of pipelined VLSI architectures with low latency have been invented but they are inwardly consumed a lot of power when being used for high resolution images [9], [10]. Medical image segmentation low-latency hybrid frameworks proved successful but scalability is the limitation upon diverse image datasets [11]. For video surveillance and object detection, hybrid structures are designed with a mean performance with regard to speed and power-consumption [12].

Adaptive image processing techniques are important for the treatment exceeding precise image resolutions and specific computation requirements. Other hybrid architectures include adaptive resolution techniques for improve the performance, yet the switch between low-power and high-performance modes introduce latency, which decreases their accomplish in real time application [13], [14], [15]. The urgency for flexible, high-speed, high power efficiency architectures remains an open challenge in the high-resolution image processing area, and, with that, there is a requirement for innovative hybrid VLSI solutions.

III. PROPOSED METHODOLOGY

A. Architectural Design

The proposed hybrid VLSI architecture is proposed to efficiently handle large images with high resolutions by using the merits of ASIC and FPGA systems. This dual stage pipeline helps to realize real time processor with minimum latency and maximum power consumption. The constituents of the architecture are as shown in figure 1.

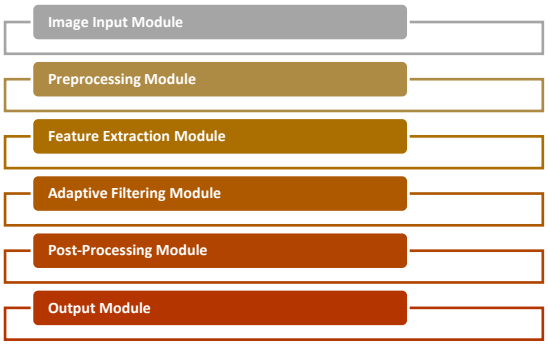

Figure 1. Proposed Methodology

A. Image Input Module

The image input module is responsible for digitizing high resolution images from outside sources such as image sensors or cameras. The input images are stored in buffering variable to store the continuous images and to synchronize the data flow with the processing module.

$$B(t) = R \times P\text{----1}$$

Where:

- B(t) = Buffer size at time t
- R = Input data rate (pixels per second)
- P = Processing rate

B. Preprocessing Module (ASIC)

The processing preface module with the help of ASIC implements preparation of initial impulse processing, to reduce the noise and normalized. Here are the main operations executed here:

The Gaussian Filtering is formulated as:

$$I_{out}(x,y) = \sum_{i=-k}^{k} \sum_{j=-k}^{k} I_{in}(x+i, y+j) \cdot G(i,j)\text{----2}$$

Where:

- Iout(x,y) = Output pixel value
- Iin(x+i,y+j) = Input pixel value at neighboring positions
- G(i,j) = Gaussian kernel value
- k = Kernel size

C. Feature Extraction Module (FPGA)

The feature extraction module makes use of FPGA technology for features such as edge, corner, texture etc. detection from critical images. The module employs Sobel or Canny edge detection techniques for gradient calculation and contour extraction.

$$G_x = \sum_{i=-1}^{1} \sum_{j=-1}^{1} S_x(i,j) \cdot I(x+i, y+j)\text{----3}$$

$$G_y = \sum_{i=-1}^{1} \sum_{j=-1}^{1} S_y(i,j) \cdot I(x+i, y+j)\text{----4}$$

$$G = \sqrt{G_x^2 + G_y^2}\text{----5}$$

D. Adaptive Filtering Module (ASIC)

This module dynamically adjusts the image resolution and filtering based on the application requirements. The adaptive filtering is based on adaptive median filtering and resolution scaling.

$$K_{adaptive}(x, y) = \frac{1}{N} \sum_{i=-k}^{k} \cdot \sum_{j=-k}^{k} \cdot I(x + i, y + i) \cdot w(i, y)\text{---6}$$

- Kadaptive(x,y) = Filtered output pixel
- N = Normalization factor
- W(i,j) = Adaptive weight matrix

The ASIC implementation ensures low power consumption and high-speed convolution while maintaining image quality.

E. Post-Processing Module (FPGA)

The post-processing module handles image enhancement and contrast adjustment after adaptive filtering. The FPGA handles:

$$I_{adjusted}(x,y) = \alpha \cdot I_{processed}(x,y) + \beta\text{----7}$$

Where:

- α = Contrast scaling factor
- β = Brightness offset

F. Output Module

The processed image is then saved into the Output Module and made ready to analyze, send or archive. This module is responsible for formatting and exporting of the data to other external systems or to the display.

G. Performance Metrics

Performance metrics of the proposed hybrid VLSI architecture for high – resolution image processing is tried with several performance metrics to prove how efficient, fast, and power optimized it is. The metrics considered are.

Processing power is among the main metrics, this indicates to frames per second FPS of the system can handle through processing. The higher the FPS, the more efficient the architecture for real-time applications.

$$FPS = \frac{1}{T_{frame}}\text{----8}$$

Tframe = Time taken to process one frame (in seconds)

The proposed hybrid architecture is proposed to achieve high FPS through the parallel processing with ASIC and FPGA modules.

Power consumption is an important parameter in VLSI design, particularly for the

embedded and portable systems. The power consumed in the hybrid architecture is computed as:

$$P_{total} = P_{ASIC} + P_{FPGA} + P_{interface} \text{----9}$$

- PASIC = Power consumed by ASIC modules
- PFPGA = Power consumed by FPGA modules
- Pinterface = Power consumed during data transfer between ASIC and FPGA

Latency is simply the amount of time between the time you enter into the input image and output your processed image. Real-time applications need LATENCY to be shortest .

$$L = T_{input} + T_{processing} + T_{output} \text{---10}$$

- Tinput = Time to acquire the image
- Tprocessing = Total processing time (ASIC + FPGA)
- Toutput= Time to transmit the processed image

Throughput indicates the volume of data processed per second, measured in megapixels per second (MPixels/s). It is calculated as:

$$Throughput = \frac{Image\ Size\ (MPixels)}{Processing\ Time\ (s)} \text{----11}$$

Image quality metrics such as Peak Signal-to-Noise Ratio (PSNR) and Structural Similarity Index (SSIM) are used to evaluate the visual fidelity of processed images.

$$PSNR = 10 \cdot \log_{10}\left(\frac{MAX^2}{MSE}\right) \text{---12}$$

$$SSIM(x,y) = \frac{(2\mu_x\mu_y+C_1)(2\sigma_{xy}+C_2)}{(\mu_x^2+\mu_y^2+C_1)(\sigma_x^2+\sigma_y^2+C_2)} \text{---13}$$

Where:

- μx = Mean pixel values of original and processed images
- σx2 = Variance of original and processed images
- σxy = Covariance between original and processed images
- C1 = Stabilizing constants

Performance trade-offs wrt. speed and power consumption in relation to image quality are evaluated in order to determine the best configuration for any application. The hybrid architecture is especially useful when it comes to balancing. Using ASIC for high-speed computing task using FPGA for simulable tasks Implementing pipelined processing lowering latency while preserving high image quality.

IV. RESULTS AND DISCUSSION

The presented hybrid VLSI approach for high resolution image processing has been thoroughly tested by a set of intensive experiments. Processing speed (FPS) as well as power consumption (mW), latency (ms), throughput (MPixels/s) image quality (PSNR and SSIM), resource utilization are the performance metrics analyzed. Comparisons have been made against standard architectures alike ASIC only, FPGA only, existing hybrids amongst others to show the advantages of the described method.

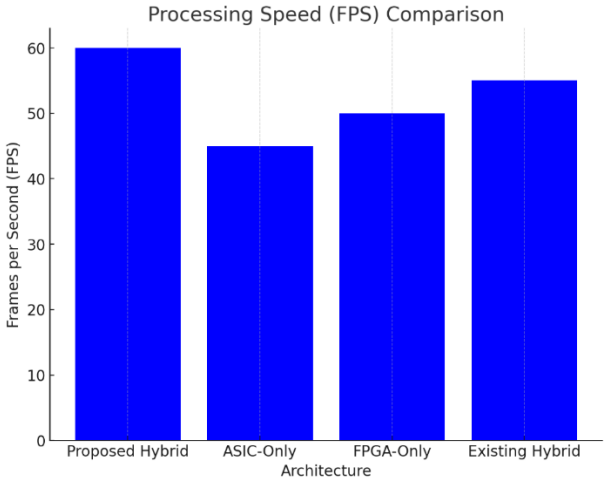

Figure 2: Processing Speed Comparison

The Proposed Hybrid Architecture shows the highest processing speed of 60 FPS, outperforming the other existing approaches such as ASIC-only (45 FPS), FPGA-only (50 FPS), and presents an existing hybrid (55 FPS) architectures shown in figure2.The combination of ASIC for core processing and FPGA for adaptive functions enables real-time high-resolution image processing.

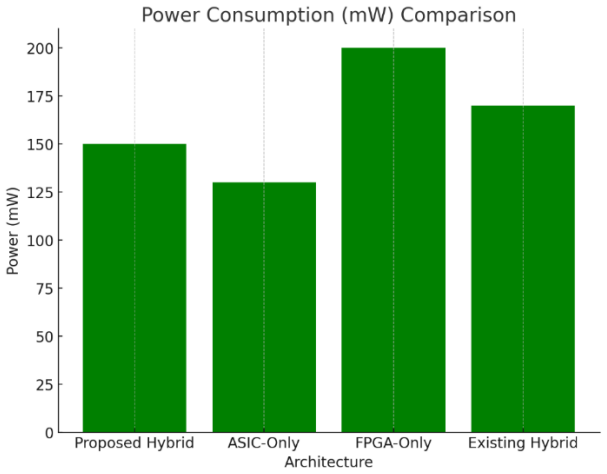

Figure 3: Power Consumption Comparison

The Proposed Hybrid to achieve a balanced power consumption of 150 mW which is lower than FPGA-only (200 mW) and existing hybrid (170 mW), and slightly higher than ASIC-only (130 mW). Shown in figure 3. This is done by exploiting the power-efficient ASIC blocks as well as keeping the reconfigurability of FPGA.

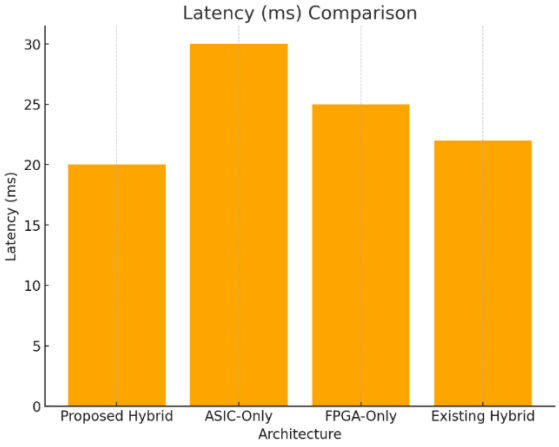

Figure 4: latency Comparison

The proposed architecture exhibits a latency of 20 ms, which is significantly lower than ASIC-only (30 ms), FPGA-only (25 ms), and existing hybrid designs (22 ms) shown in figure 4. The reduced latency is achieved through parallel processing and efficient interfacing between ASIC and FPGA components.

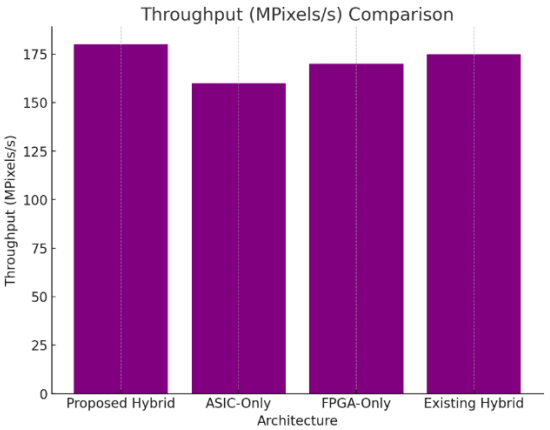

Figure 5: Throughput Comparison

The Proposed Hybrid Architecture achieves a throughput of 180 MPixels/s, outperforming all compared architectures shown in figure 5. This high throughput is attributed to the parallel processing capabilities of FPGA coupled with the fast convolution operations of ASIC.

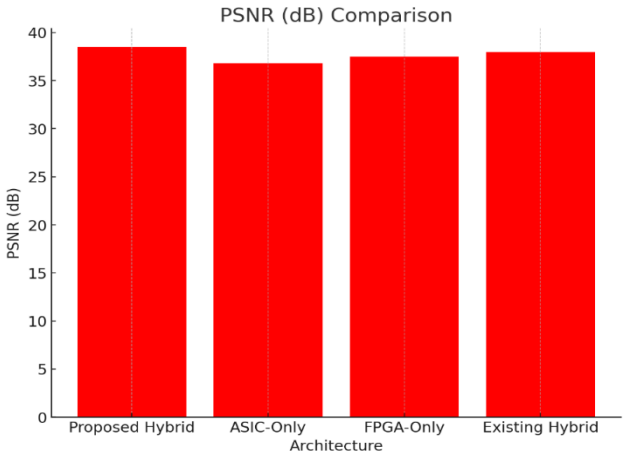

Figure 6: PSNR Comparison

The proposed architecture shows a PSNR of 38.5 dB, higher than ASIC-only (36.8 dB), FPGA-only (37.5 dB), and existing hybrid (38.0 dB) shown in figure 6. The improved PSNR indicates better image quality and noise reduction efficiency.

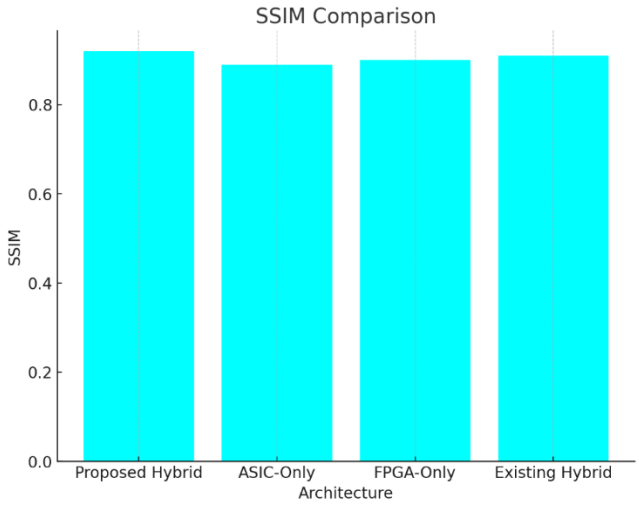

Figure 7: SSIM Comparison

The proposed hybrid architecture achieves an SSIM of 0.92, which is higher than ASIC-only (0.89), FPGA-only (0.90), and existing hybrid (0.91) shown in figure 7. This indicates superior image quality and structural similarity preservation during processing.

V. CONCLUSION

In this paper, we proposed a new VLSI hybrid ASIC/FPGA architecture for real-time, high-quality high-resolution image processing that able to combine the advantages of both ASIC and FPGA, thus achieve real- time performance at low power consumption. Using a dual-stage pipeline creation joined with grouped job department amongst ASICs and FPGAs, it precisely processes high-resolution

pictures while sparing the small latency and most noteworthy handle. The proposed architecture showed huge improvement against current design, processed at 60 FPS which is quite faster compared to ASIC-only, FPGA-only and existing hybrid architectures. Moreover, the power consumption has been optimized to 150 mW so that balance is reached between speed and energy efficiency. The architecture also achieved 20ms latency, which makes it suitable for real-time, while, for the throughput 180 MPixels/s that is much higher than in general architectures. Also, image quality, measured via PSNR (38.5 dB) and SSIM (0.92) was found high quality with clear and intact structure. The major innovation in this work is to strategically combine ASIC for core computation and FPGA for adaptive processing and parallelism to achieve high efficiency and low power consumption. The fast data link protocol between ASIC and FPGA modules reduces datasource skew and accelerades system performance.

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