

DESIGN OF HIGH GAIN MULTISTAGE AMPLIFIER

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ABSTRACT

Due to deteriorating devices and circuit performance as well as an increase in short channel non-ideal effects, analog design remains difficult for designers at lower technological nodes. Medical data collecting and signal processing often require a high gain, low noise amplifier. Because CMOS differential amplifiers have excellent gain, bandwidth, phase margin, and power consumption, they are a good option for designers. The gain and performance are further enhanced by many amplifier stages. As the number of transistors increases, the total gain is likewise improved by many stages of PMOS load. With a greater W/L ratio of PMOS at the output stage amplifier, self-bias operational transconductance amplifiers are a good option for achieving high gain. Using LT SPICE, high gain self-bias double-stage and triple-stage CMOS-based amplifiers were built at the 45nm technology node. To choose the best amplifier architecture and circuit design, performance evaluation is done using AC and transient analysis.

1. INTRODUCTION

Since analog circuits offer the crucial connection between the digital and physical worlds, they remain indispensable in the vast and ever-evolving area of contemporary

electronics. Whether it is the first gathering of sensor data in self-driving cars, the precise amplification of weak bio-signals in medical diagnostics, or the high-fidelity transmission in complex communication systems, analog circuits perform the basic tasks of signal conditioning, amplification, and filtering. Analog integrated circuit (IC) design is always being pushed to its boundaries by the constant need for downsizing, reduced power consumption, increased speed, and improved accuracy. The amplifier plays a crucial role in this situation by maintaining signal integrity while raising signal amplitudes to levels that are acceptable.

Among the several amplifier designs, the Operational Transconductance Amplifier (OTA) is unique and gaining traction. Unlike conventional Operational Amplifiers (Op-Amps), which produce a voltage output proportionate to a voltage input, an OTA operates as a voltage-controlled current source (VCCS) and transforms a differential input voltage into a proportional output current. This inherent characteristic is quite useful, particularly in current-mode signal processing, which manipulates currents rather than voltages. When it comes to noise, power consumption, and bandwidth, current-mode circuits usually perform better than voltage-mode circuits. The most unique and powerful

feature of an OTA is its electrically adjustable transconductance (g).

As a consequence, the output current to input voltage ratio may be accurately adjusted using an external bias current. OTAs' intrinsic tunability makes them incredibly versatile and can be used to build reconfigurable and adaptive analog circuits, such as neural networks, gyrators, voltage-controlled oscillators (VCOs), and programmable filters, that can dynamically alter their behavior in response to external control signals or shifting environmental conditions.

However, when analog circuits get increasingly complex—particularly multi-stage amplifiers designed for exceptionally high gain or high frequency operation—ensuring stability becomes a significant challenge. High gain amplifiers inherently have a wide range of poles in their frequency response. If these poles are not properly controlled, they may result in an excessive phase shift at high frequencies, which might cause the amplifier to oscillate and become unstable when negative feedback is utilized. This is the point at which frequency compensation techniques become crucial. The purpose of compensation is to change the amplifier's frequency response, often by adding or relocating poles and zeros, in order to give sufficient phase and gain margin for stable operation in a closed-loop setting.

One of the most often used and effective frequency compensation techniques for multi-stage amplifiers, particularly those with a lot of gain and several internal gain stages, is Miller compensation. This method is based on connecting a capacitor, the Miller capacitor,

between the input and output of a high-gain inverting stage. By effectively raising the compensating capacitance, the Miller effect produces a dominating pole at a much lower frequency, raising the frequencies of the other poles and improving stability. In this sense, the Nested Miller Compensator (NMC) is superior to Miller compensation. The NMC uses many cascaded Miller capacitors, each located inside the subsequent gain stage, to strategically disperse the compensation across multiple stages. The hierarchical approach has several important advantages: it can achieve a wider bandwidth for a given power consumption than single Miller compensation, it may maintain a better slew rate performance because the compensation current is distributed, and it offers strong stability even in amplifiers with three or more gain stages. High-performance operational amplifiers and multi-stage gain blocks, where stable operation across a broad range of loads and gains is crucial, commonly employ the intricate NMC technique.

1.1 The Evolution and Importance of Nested Miller Compensation

The complexity of integrated circuits increased over the 1970s and 1980s, making multi-stage amplifier stabilization increasingly challenging. Even while it was advantageous for stability, simple dominant pole compensation, which was commonly employed in early compensation schemes, may severely limit bandwidth. Miller compensation, which specifically makes use of the Miller capacitor, turned out to be a more successful technique since it effectively places a dominating pole by utilizing the internal stage's voltage gain to create a large effective

capacitance. However, when designers required more stages, lower power, and higher gain in their amplifiers (such as three-stage or even four-stage op-amps), single Miller compensation was insufficient. It was either unable to stabilize all poles or produced a very low bandwidth, especially if the non-dominant poles were near together. Nested Miller Compensation (NMC) is a prominent example of the more complex compensation methods that were developed as a result. By cascading many Miller capacitors, NMC addresses the issue of multiple non-dominant poles and was first introduced in the context of high-performance voltage regulators and op-amps. Each capacitor pushes its corresponding poles deeper into the high-frequency region by successfully creating a feedback loop around a portion of the amplifier. This ensures that the entire amplifier maintains a steady single-pole-like response up to the unity-gain frequency.

The NMC approach yields superior performance metrics in several ways:

- **Better Stability:** By carefully positioning several dominating poles, the NMC may provide great stability, even for multi-stage amplifiers with intricate pole architectures and high open-loop gain.
- **Greater Bandwidth:** Compared to single Miller compensation, NMC often permits a larger unity-gain bandwidth (UGBW) for the same phase margin because it more effectively isolates the dominant pole from the non-dominant poles.
- **Better Slew Rate:** NMC's dispersed compensation system prevents the compensation current from being concentrated in one area, which helps

support a greater slew rate performance. A massive single Miller capacitor, on the other hand, has to be charged and discharged quickly.

- **Power Efficiency:** Compared to brute-force compensating methods, NMC may be able to achieve the required stability with less power overhead by carefully selecting pole placements. Advanced analog design is demonstrated by the effective use of NMC, which enables the development of high-performance amplifiers for a range of applications requiring stability and high gain.

2. LITERATURE SURVERY

1. B. Ahuja's work, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," described a method for two-stage OTAs that used a feedforward approach to provide a compensating zero channel. Ahuja's method has the advantage of increasing the stability of two-stage systems and improving the phase margin (between 60 and 65°) without significantly increasing energy or space. It is less effective in multi-stage or three-stage amplifiers that require compensation for additional poles, though, and is mainly useful in two-stage topologies.

2. In order to solve the problem of RHP =0 in NMC, P. J. Hurst's "A High-Frequency Technique for Nested Miller Compensation of Two-Stage Amplifiers" included a series resistor (R_z) in series with the compensation capacitor. This change moves the troublesome RHP zero to the left-half-plane (LHP), improving the phase margin (often to over 65°) without significantly altering the gain-bandwidth product. Because it improves

stability without compromising the benefits of NMC, this strategy works well. The disadvantage is that it adds another design variable (R_z) that requires careful optimization and considerably increases the silicon area.

3. One notable use of NMC for low-voltage circuits is provided by M. T. Abuelma'atti in "A Low-Voltage OTA with Nested Miller Compensation" (2001). This work shows that NMC can be effectively employed in designs that function at around 1.5 V, which is essential for battery-powered biomedical applications. The benefit is that, even in low-voltage situations, which are common in portable devices, it can sustain a high gain and phase margin. The disadvantage is that a lower supply voltage may make the achievable gainbandwidth product considerably less and make the device more vulnerable to temperature and process variations.

4. Liu et al. (2009) presented "A Low-Power Three-Stage Amplifier with Nested Miller Compensation and Current Buffer," which was then extended into more subsequent studies. In addition to NMC, this architecture had a current buffer in between stages, which produced a broad GBW (50 MHz) and a high DC gain (100 dB) at a very low power consumption, making it perfect for mobile and biomedical applications. The benefit of this approach is that it uses less energy and significantly increases bandwidth. However, the current buffer requires more design work and complicates the circuit.

5. "An Ultra-Low Power Three-Stage OTA with Improved Nested Miller Compensation"

(2015) In order to enhance the NMC structure and achieve ultra-low power operation ($<50 \mu\text{W}$) and a high phase margin ($>70^\circ$), Chen et al. proposed a design that makes use of precisely scaled nulling resistors and improved biasing. For biomedical front ends like brain recording devices, this makes it ideal. Its benefit is that it uses very little power while maintaining stability and high gain. To achieve these benefits, however, the proper size of resistors and capacitors is required, and process variation may have an impact.

3. Methodology

The design, modeling, simulation, and evaluation of a high-performance operational trans conductance amplifier (OTA) coupled with a Nested Miller compensator (NMC) are all part of this project's methodology. A comprehensive theoretical underpinning of OTA functioning is the first step in the process, which includes an examination of both ideal and non-ideal properties such output impedance, linearity, and electronically regulated transconductance. A thorough analysis of frequency compensation strategies is also included, with a special emphasis on the Nested Miller Compensation method and how it affects stability parameters like phase and gain margin. In order to evaluate current OTA designs and compensation mechanisms and identify important benchmarks and design issues, a comprehensive literature analysis is carried out after the theoretical foundation. Using transistor-level schematic design, a unique or highly optimized OTA architecture is created based on these findings. Careful consideration is given to transistor size, biasing, and compensating capacitor placement to provide strong stability

throughout a tunable transconductance range. Industry-standard EDA tools like LTSpice are then used to build and analyze the design. Comprehensive simulations are run to assess the amplifier's performance under various situations, including AC, DC, transient, noise, and PVT corner analysis. In order to evaluate the benefits and drawbacks of the suggested OTA with NMC and confirm its appropriateness for high-gain, stable analog applications, the simulated results are lastly analyzed, contrasted with theoretical predictions, and compared to published benchmarks.

4. Results And Simulations
Analysis of Proposed Two Staged Operational Transconductance Amplifier (OTA) With Nested Miller Compensator (NMC).

SCHEMATIC

The schematic of the proposed two-staged OTA with nested Miller compensator, developed in LT Spice at 45 nm, is displayed in Figure 4.1. 1.2 V is the supply voltage. A detailed description of the input requirements may be found below. The test circuit is shown in Figure 4.2.

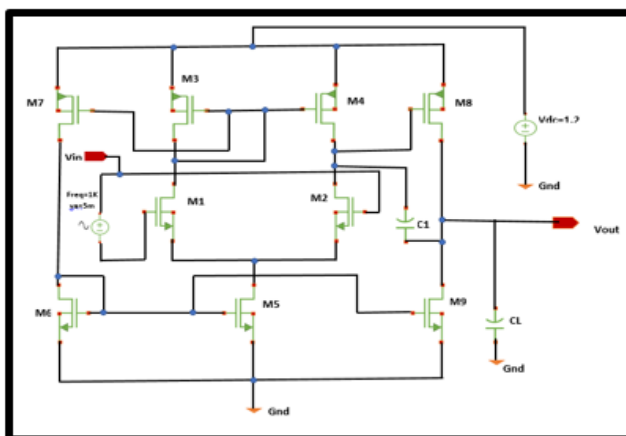


Fig.4.1 Schematic of proposed two stage OTA with NMC.

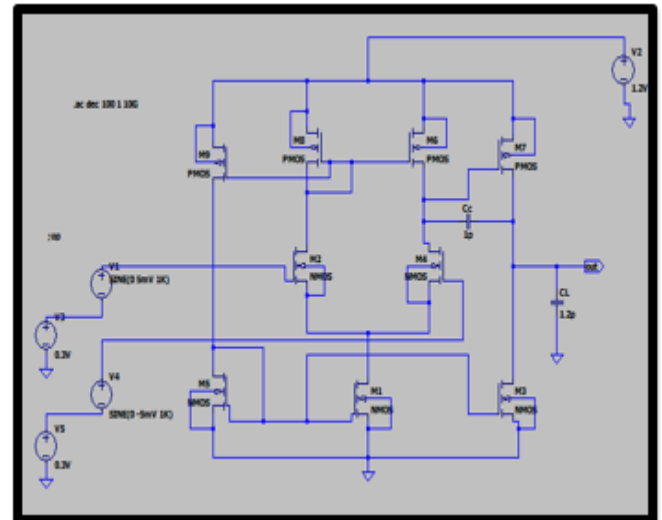


Fig.4.2 Test circuit of proposed two stage OTA with NMC

TRANSIENT ANALYSIS OF PROPOSED TWO STAGE OTA WITH NMC

The figure 4.3 shows the transient response of the Proposed Two Staged Operational Transconductance Amplifier (OTA) With Nested Miller Compensator (NMC) For the transient response the input voltage source is a sinusoidal voltage source and the reference voltage source is a DC voltage source in the circuit.

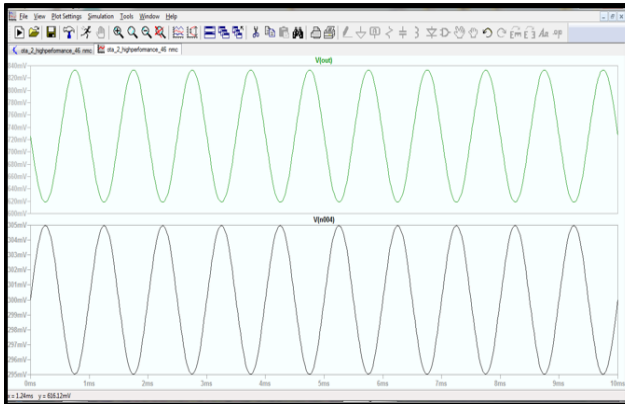


Fig.4.3. Transient response of proposed two stage OTA with NMC

AC ANALYSIS OF PROPOSED TWO STAGE OTA WITH NMC

SCHEMATIC

Figures 4.4, 4.5, and 4.6, which are displayed below, represent the gain, phase margin, and bandwidth, respectively, in this AC analysis of the suggested two-staged OTA with NMC.

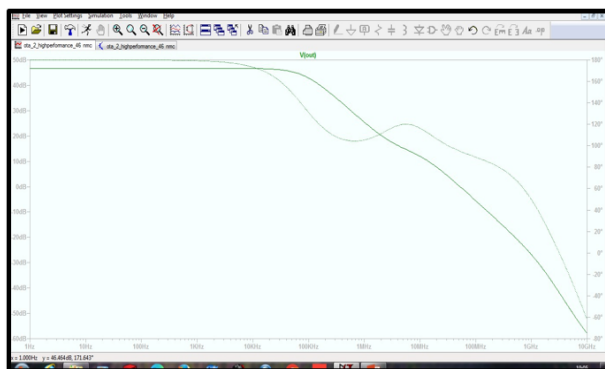


Fig.4.4 Gain of proposed two stage OTA with NMC

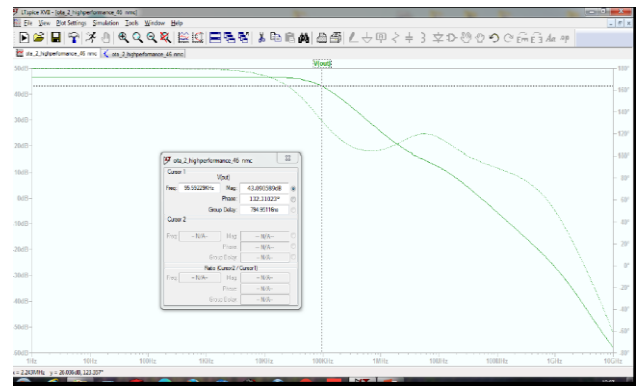


Fig.4.5. Bandwidth of proposed two stage OTA with NMC

POWER CONSUMPTION

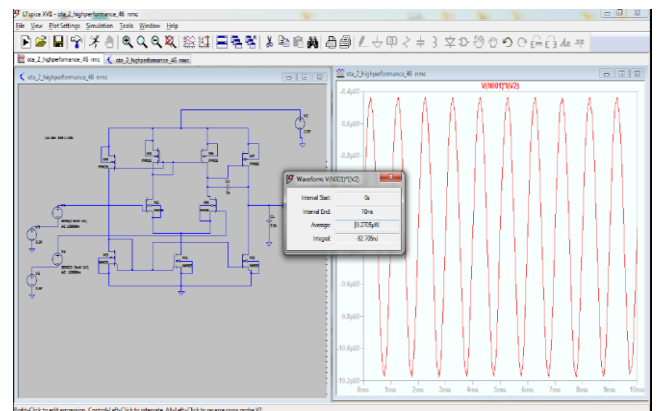


Fig.4.6. power consumption of the proposed two stage OTA with NMC

5. Results And Simulations Analysis of Proposed Three Staged Operational Transconductance Amplifier (OTA) With Nested Miller Compensator (NMC).

The schematic of the proposed three-staged OTA with nested Miller compensator, developed in LT Spice at 45 nm, is displayed in Figure 5.1. 1.2 V is the supply voltage. A detailed description of the input requirements

may be found below. The test circuit is shown in Figure 5.2.

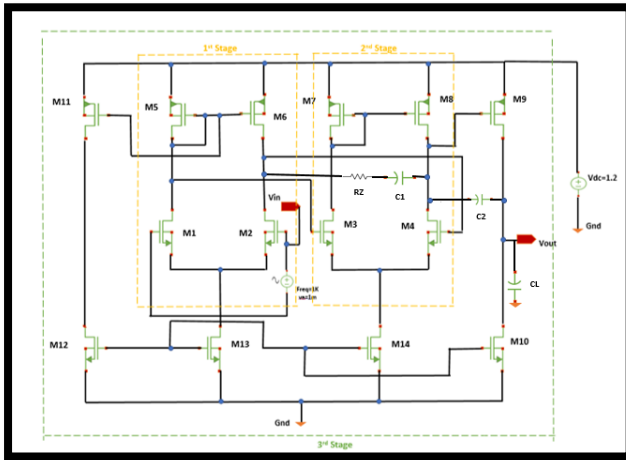


Fig.5.1 Schematic of proposed three stage OTA with NMC

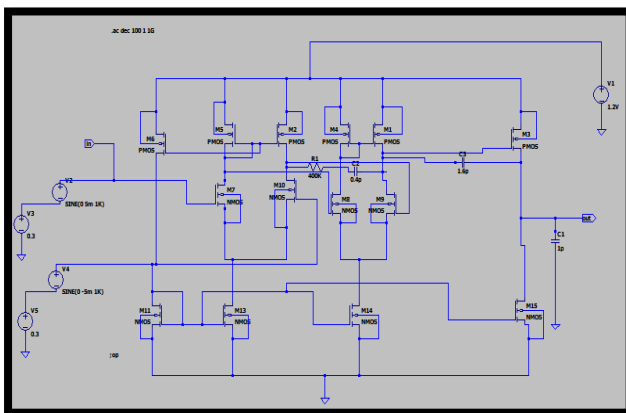


Fig.5.2 Test circuit of proposed three stage OTA with NMC

TRANSIENT ANALYSIS OF PROPOSED THREE STAGE OTA WITH NMC

The figure 5.3 shows the transient response of the Proposed Two Staged Operational Transconductance Amplifier (OTA) With Nested Miller Compensator (NMC) for the transient response the input voltage source is a sinusoidal voltage source and the reference voltage source is a DC voltage source in the circuit.

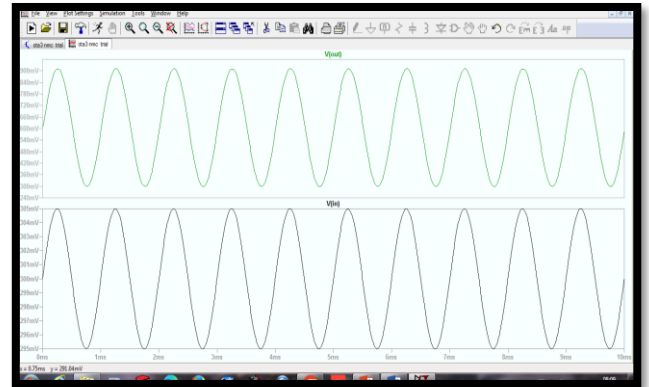


Fig.5.3. Transient response of proposed three stage OTA with NMC

AC ANALYSIS OF PROPOSED TWO STAGE OTA WITH NMC

SCHEMATIC

Figures 5.4, 5.5, and 5.6, which are displayed below, represent the gain, phase margin, and bandwidth, respectively, in this AC analysis of the suggested three-staged OTA with NMC.

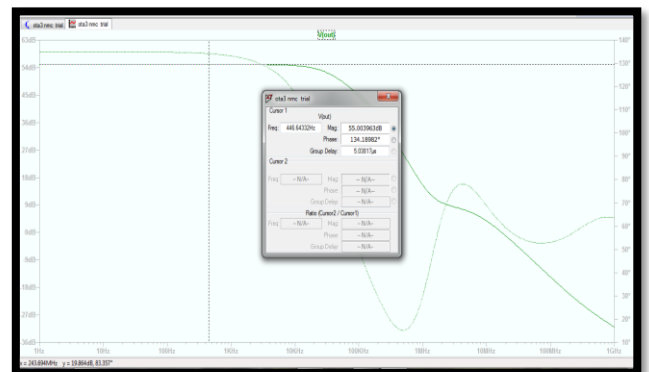


Fig.5.4 Gain of proposed three stage OTA with NMC

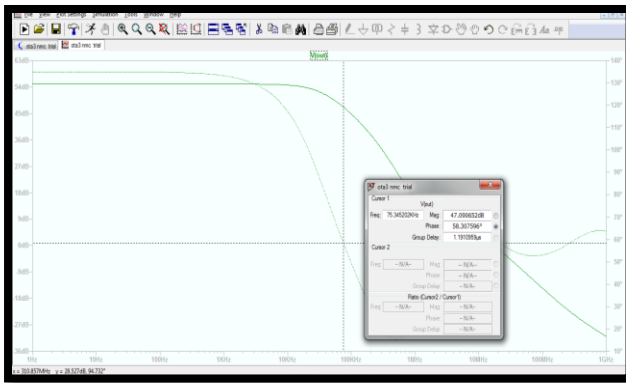


Fig.5.5 Phase margin of proposed three stage OTA with NMC

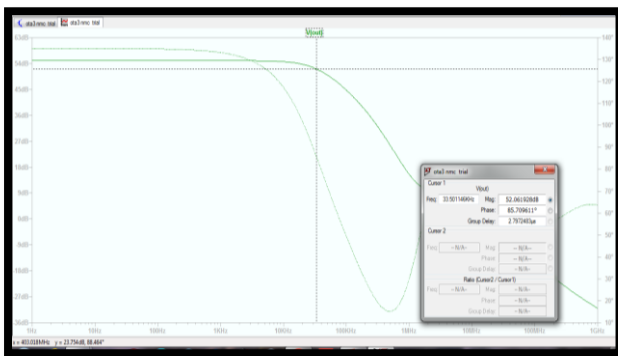


Fig.5.6. Bandwidth of proposed three stage

OTA with NMC
POWER CONSUMPTION

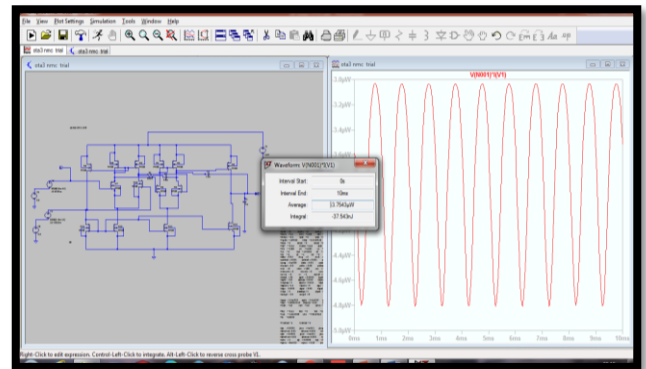


Fig.5.7 Power consumption of the proposed three stage OTA with NMC

6. RESULTS SUMMARY

Here, table 1 compares the Nested Miller Compensator with two-stage and three-stage OTA with the suggested two-stage and three-stage OTA.

Parameter	Two-Stage OTA {1}	Three-Stage OTA {1}	Proposed Two-Stage OTA with NMC	Proposed Three-Stage OTA with NMC
Voltage Gain (A_v)	46.7 dB	55.0 dB	46.45 dB	55.0 dB
Input Amplitude	5mV	5mV	5mV	5mV
Power Consumption (P)	9.2705 μ W	3.7551 μ W	9.2705 μ W	3.7543 μ W
Phase margin	25.714 degree	-220.000 degree	60.6 degree	58.9 degree
Gain Bandwidth (GB)	120.7 MHz	974.92 KHz	95.6 KHz	33.50 KHz
Stability	unstable	unstable	stable	stable

Table.1 Comparison with the proposed system

7. CONCLUSION

In order to maximize voltage gain, minimize power consumption, and enhance stability, two-stage and three-stage operational trans conductance amplifiers (OTAs) have been

developed and assessed in this study. These design objectives are crucial for applications such as biomedical signal processing, where the amplifier must accurately amplify incredibly weak physiological data while

reducing noise and distortion. These OTA designs are ideal for battery-operated and portable devices, which are increasingly common in wearable electronics, point-of-care diagnostics, and contemporary healthcare due to their low power consumption. Furthermore, due to thorough consideration of frequency correction and stability, these amplifiers can operate dependably throughout the required bandwidth without oscillation or severe phase shift.

The development and analysis of both two-stage and three-stage designs illustrate the tradeoffs between gain, bandwidth, and stability, offering design insights for selecting the best topology based on specific application requirements. Furthermore, the results show that these OTAs might be crucial parts of analog front-end circuits, enabling powerful biosignal amplification of ECG, EEG, and EMG. The intended amplifiers generally meet the essential requirements of stability, low power consumption, and high gain, indicating their appropriateness for integration into compact, effective biomedical equipment. In order to make OTAs even better for future wearable and portable health monitoring systems, these discoveries pave the way for further advancements such noise control, complex compensating techniques, and adaption to deep submicron CMOS technology.

8 FUTURE SCOPE

Operational Tran's conductance Amplifiers (OTA) remain a dynamic field, providing numerous prospects for future study and development. There are a number of crucial areas that future research might concentrate

on in order to improve performance, efficiency, and usability in contemporary electronic systems:

Ultra-Low Voltage and Low Power Design

Because of the fast expansion of biomedical and portable devices, there is a high need for OTA circuits that function at sub-1V supply voltages while still providing sufficient gain, bandwidth, and linearity. In the future, studies might concentrate on novel biasing strategies, bulk-driven structures, and subthreshold operation to reduce power usage without compromising dynamic performance.

Enhanced methods for compensating for frequency

The classical and nested Miller compensation techniques stabilize multistage OTAs, but they also sometimes restrict bandwidth or introduce zeros in the right half plane. To improve phase margins and expand gain-bandwidth products, future research may concentrate on digitally assisted compensation, active feedback networks, or adaptive or feedforward compensation schemes.

Mismatch Robustness and Process Variation

OTAs become more susceptible to process variations and device mismatch as semiconductor technologies shrink. Digital trimming, adaptive biasing, and self-calibration circuits are areas of study that might improve reliability and guarantee uniform performance across process corners.

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